Introduction

This application note discusses the design of an HFA1155 based amplifier for gains ≥2, in a single 5V supply application.

Table 1 shows the typical performance data for the HFA1155 with a 5V supply and R_L = 500Ω. Note that the HFA1150 should be used for single 5V applications with $R_L < 500$Ω, as the HFA1155 doesn't have the drive capability at this low supply voltage. The two most important parameters that determine the design configuration are the Common Mode Input Range (CMIR) and the Output Voltage Swing. Violating either of these two specifications jeopardizes the design, and may prevent the user from achieving the performance listed in the rest of the table.

Biasing the Amplifier for Gains ≥2

Obviously, using a non rail-to-rail op amp in single supply applications requires that the amplifier input and output be biased in their useful range, typically to 2.5V for a 5V application. One way to accomplish this is to sum the bias voltage into the feedback network. Unfortunately, the bias voltage sees an inverting gain, so the required positive output offset voltage requires a negative input bias voltage, something not usually available in single 5V systems.

A simple approach for solving the biasing problem utilizes AC coupling (see Application Note AN9757 for a discussion of DC coupled approaches) to superimpose the AC input signal on the desired DC bias voltage. A bias network on the op amp side of the coupling capacitor generates the voltage required to properly position the op amp input and output within the useful range.

Using a High Impedance Bias Network

The circuit in Figure 1 biases the op amp input and output at 2.5V to take full advantage of the HFA1155's CMIR and output swing capability. To properly center the input signal within the op amp's CMIR, C_1 is needed to remove the input signal DC component, while the resistor divider formed by R_2 and R_3 establish the new DC reference of 2.5V. Choosing 5kΩ for R_2 and R_3 keeps the bias network current small (i.e., $I_{BIAS} = 5/(R_2 + R_3)$ = 0.5mA), and minimizes the load on the input signal source. Note that the 50Ω source termination resistor, if

required, is placed on the source side of C_1. C_2 AC grounds the op amp's feedback network, which ensures that all DC voltages at the op amp's noninverting input (e.g., the bias voltage) see a gain of 1. C_2 is a short for high frequencies, so the AC input signal gets the desired gain of $1+R_5/R_4$.

Without C_2 (i.e., DC grounding the feedback network) the DC and AC components both get amplified by $1+R_5/R_4$, which presents an interesting challenge of trying to bias both the input and the output within the allowed range, especially at high gains. Consider a circuit with a desired signal gain of 5. Centering the output at the desired 2.5V midpoint, requires biasing the noninverting input at 0.5V - clearly a violation of the CMIR spec. With C_2 utilized, the DC and AC gains are independent, so large AC gains are easily implemented.

As usual, there is a cost associated with the implementation. The large value bias resistors increase the amplifier's output offset voltage (V_{OS}) and low frequency noise level. The op amp's input current (I_B) flows through the bias network creating an offset voltage that gets amplified by the DC gain, so $V_{OS} = I_B*(R_2||R_3)*A_{VDC}$ = 25µA*2.5kΩ*1 = 63mV. Likewise, the amplifier's input noise current interacts with the bias resistors - and C_1's impedance - to generate a noise voltage which gets amplified by the amplifier's AC gain. Fortunately, C_1's impedance dominates (and reduces) the effective source impedance ($Z_{C1}||R_2||R_3$) value by 2kHz, which is significantly before Z_{C2} has much impact on increasing the AC gain.

Using a Low Impedance Bias Network

The circuit in Figure 2 minimizes the offset voltage and low frequency noise increases associated with the previous approach. The operation of this circuit is essentially the same as Figure 1, except that a low output impedance DC supply provides the 2.5V bias voltage. R_1 provides the 50Ω source termination and C_2 provides a good AC ground at the bias voltage. The low impedances of R_1 and the bias voltage supply minimize the offset voltage and low frequency noise contributions compared to the large bias resistors used in Figure 1.

Figures 3 and 4 illustrate the pulse and frequency responses for the HFA1155 in the two circuits discussed above.

TABLE 1. HFA1155 SINGLE 5V PERFORMANCE DATA WITH R_L = 500Ω

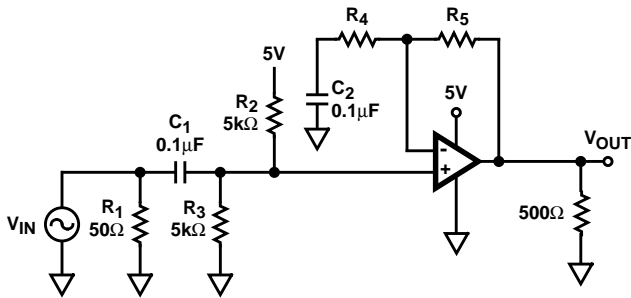| PARAMETER	TYPICAL VALUE (SOIC, R_F = 1.5kΩ)	TYPICAL VALUE (SOT-23, R_F = 1.15kΩ)
Common Mode Input Range	1V to 4V	1V to 4V
-3dB BW (A_V = +2)	130MHz	130MHz
Gain Flatness (to 50MHz, A_V = +2)	±0.1dB	±0.07dB
Output Voltage (A_V = -1)	1V to 4V	1V to 4V
Slew Rate (A_V = +2)	160V/µs	160V/µs
0.1% Settling Time	55ns	55ns
Supply Current	1.4mA	1.4mA

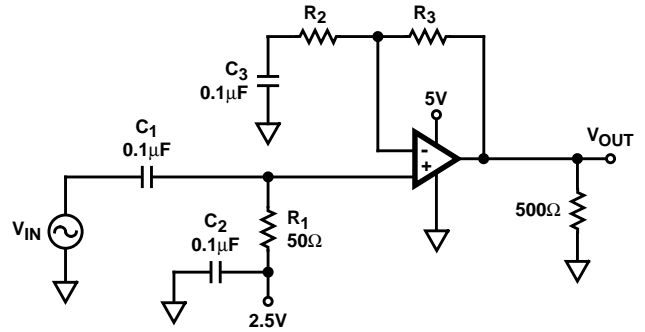FIGURE 1. HFA1155 WITH A_V = +2 AND A HIGH IMPEDANCE BIAS NETWORK

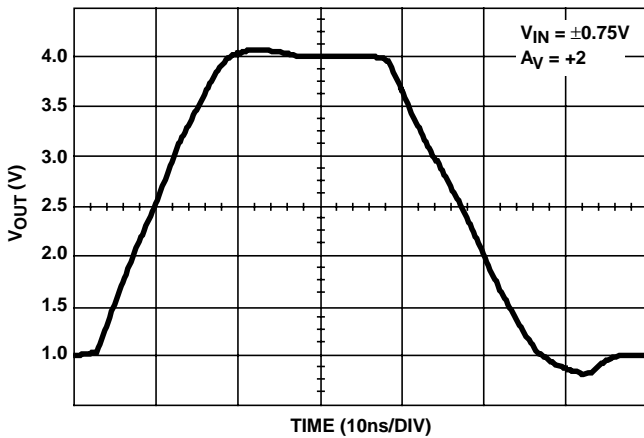FIGURE 2. HFA1155 WITH A_V = +2 AND A LOW IMPEDANCE BIAS NETWORK

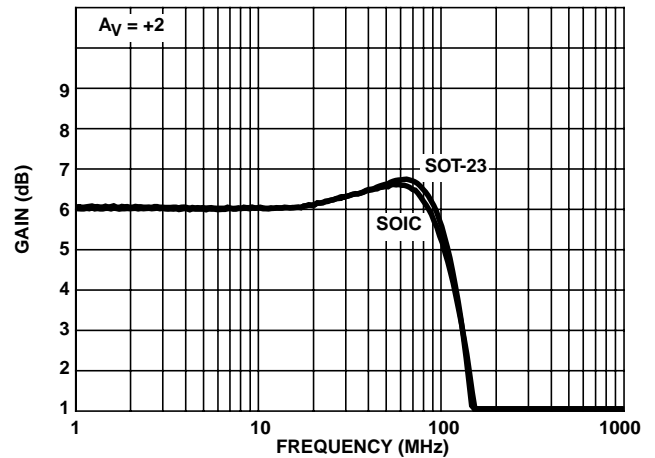FIGURE 3. HFA1155 TRANSIENT RESPONSE FOR CIRCUITS IN FIGURES 1 AND 2

FIGURE 4. HFA1155 FREQUENCY RESPONSE FOR CIRCUITS IN FIGURES 1 AND 2

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